



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,055	07/29/2003	Wayne Kever	10016669-3	5930

7590 11/16/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER

BEREZNY, NEMA O

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/629,055	KEVER, WAYNE
	Examiner	Art Unit
	Nema O Berezny	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 29 July 2003.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 23-33 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 23-33 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 29 July 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

This Office Action is in response to Applicant's Amendment filed 7-29-03, which has been entered and considered. Claims 23-33 are currently pending; cancellation of claims 1-22 is acknowledged.

Applicant's Amendment of corrections to the drawings and specification is acceptable to Examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 23-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In independent claim 23, it is uncertain what is being claimed in lines 9-11, in particular the portion claiming "... by virtue of omission of a solder bump ...". Correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 23-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Eldridge et al. (2001/0052786). Eldridge discloses an integrated circuit device, comprising: an integrated circuit die having a plurality of solder pads used for conveying signals to and from the die, the integrated circuit having a plurality of blocks of circuitry; a substrate having a plurality of solder pads corresponding to at least a portion of the integrated circuit die's solder pads; a plurality of solder bumps connecting the substrate to the integrated circuit die; and wherein at least one of the blocks of circuitry is configured by virtue of omission of a solder bump for at least one connection between the substrate and the at least one of the plurality of blocks of circuitry (Figs.1, 3A, 6, 9; p.3 para.49; p.4 para.55,58; p.5 para.70) **[claim 23]**. Eldridge also discloses wherein the at least one of the plurality of blocks of circuitry is disabled by omission of a solder bump that supplies power supply voltage to the at least one of the block of circuitry (p.3 para.53) **[claim 24]**; wherein the block of circuitry that is disabled is identified by testing the plurality of blocks of circuitry for functionality (p.3 para.53) **[claim 25]**; wherein the block of circuitry that is disabled is determined to not be functional by said testing (p.3 para.53) **[claim 26]**; wherein the block of circuitry that is disabled comprises one of a plurality of microprocessor cores (p.2 para.43) **[claim 27]**; wherein the block of circuitry that is disabled comprises at least one of a plurality of memory blocks (p.2 para.43) **[claim 28]**; wherein the block of circuitry that is disabled

comprises one of a plurality of redundant blocks of circuitry (p.4 para.65) [claim 29]; wherein one of the plurality of solder bumps connects the substrate to a ground node in the block of circuitry that is disabled (p.3 para.53) [claim 30]; wherein the omitted solder bump, if present, would connect the substrate to a logic input forming a part of the block of circuitry (p.2 para.43) [claim 31]; wherein the substrate forms part of a chip carrier (p.4 para.55) [claim 32]; and wherein the one of the plurality of blocks of circuitry is configured by selective connection of a signal to a logic gate (p.5 para.67) [claim 33].

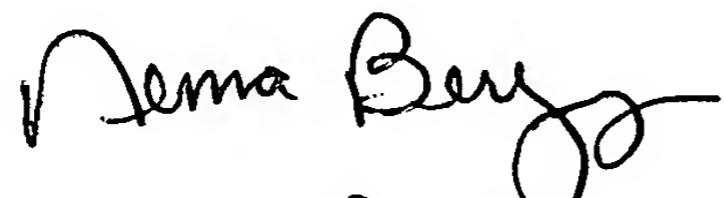
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB


Nema Berezny